REMARKS

This communication is filed in response to the Office Action having a mailing date of December 18, 2009, in which a three (3) month Shortened Statutory Period for Response has been set, due to expire March 18, 2010. Twenty-three (23) claims, including three (3) independent claims, were paid for in the application. Claims 1, 6, 10, and 23 are currently amended. Claim 5 is canceled, and claim 6 is amended only to depend from amended claim 1. No new matter has been added to the application, and all claims are believed in condition for allowance. Upon entry of the amendments herewith, claims 1-3 and 6-23 are pending. Reconsideration of the present application in view of the following remarks is respectfully requested.

I. Rejections under 35 U.S.C. § 103(a)

The final Office Action maintained rejections of all claims under 35 U.S.C. § 103(a) as allegedly unpatentable over *Wang et al.*, **(U.S. Appl. 2002/0116565)**, hereinafter *Wang*, in view of *Hamdi et al.*, **(U.S. Pat. 6,912,651)**, hereinafter *Hamdi*.

Claim 1 has been amended to recite, *inter alia*, "said first section of the internal memory is sub-divided into two sub-parts, and is adapted to consecutively store transfer descriptor headers relating to periodic transfers in a first subpart, and to consecutively store transfer descriptor headers relating to asynchronous transfers in a second sub-part."

Claim 10 has been amended to recite, *inter alia*, "the internal memory having a first section adapted to consecutively store transfer descriptor headers and a second section adapted to consecutively store transfer descriptor payloads, the first section sub-divided into a first subpart adapted to consecutively store transfer descriptor headers relating to periodic transfers and a second subpart adapted to consecutively store transfer descriptor headers relating to asynchronous transfers."

Claim 23 has been amended to recite, *inter alia*, "configuring a block of dedicated transfer descriptor payload address space of an internal memory to be mappable in the host microprocessor, wherein said address space accessible via the memory bus, wherein the block of dedicated transfer descriptor header address space is separate from the block of dedicated

transfer descriptor payload address space, and wherein the block of dedicated transfer descriptor header address space is sub-divided into a first subpart adapted to consecutively store transfer descriptor headers relating to periodic transfers and a second subpart adapted to consecutively store transfer descriptor headers relating to asynchronous transfers."

Support for the amendments is found in the present application at least in Figures 2-4 and Page 3, Lines 23-28, which lines correspond to paragraph [0027] of the present publication. Said lines, reproduced for convenience with emphasis added, recite:

> As shown in FIG. 4, the RAM is effectively divided into two parts, namely a first part **70** which contains header and status information for the stored transfer descriptors TD **1** , TD **2** , . . . , TDn, and <u>which is itself subdivided into a portion 72 relating to asynchronous (bulk) transfers and a portion 74 relating to periodic (isochronous and interrupt) transfers</u>, and a second part **76** , which contains the payload data for those stored transfer descriptors TD **1** , TD **2** , . . . , TDn

Subsequent parts of the detailed description of the present application indicate that such partitioning in the memory of the host controller permit the host microprocessor to easily write and read all of the transfer descriptor headers together. See, for example, Page 3, Lines 29-33, which lines correspond to paragraph [0028] of the present publication. Other parts of the detailed description describe how the host controller memory is memory mapping in the host microprocessor. See, for example, Page 4, Lines 16-20, which lines correspond to paragraph [0034] of the present publication.

Neither *Wang* nor *Hamdi* disclose, teach, or suggest the features described in the independent claims. Accordingly, the rejections are traversed and the claims are in condition for allowance.

II. Conclusion

Overall, none of the references singly or in any motivated combination disclose, teach, or suggest what is recited in the independent claims. Thus, given the above amendments and accompanying remarks, the independent claims are now in condition for allowance. The dependent claims that depend directly or indirectly on these independent claims are likewise allowable based on at least the same reasons and based on the recitations contained in each dependent claim. If the attorney of record (Thomas J. Satagaj) has overlooked a teaching in any of the cited references that is relevant to the patentability of the claims, the Examiner is requested to specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact Mr. Satagaj at (206) 622-4900.

The Director is authorized to charge any additional fees due by way of this Amendment only, or credit any overpayment, to our Deposit Account No. 19-1090. Reconsideration of the present application in view of the foregoing amendments and the following remarks is respectfully requested. A Notice of Allowance is earnestly solicited.

Respectfully submitted,

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